Fraunhofer Institut Photonische Mikrosysteme

Multiline Passive Matrix OLED Driver ASIC

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The newly developed passive-matrix OLED (PMOLED) driver ASIC (Application-Specific Integrated Circuit) was specifically designed for evaluating advanced OLED driving schemes as multi-line or optimized single line driving for highly reliable displays. The ASIC is capable of driving up to 4 lines at the same time in random order. This allows larger and/or brighter PM OLED displays as well as longer lifetimes and increased energy efficiency.

Passive-matrix driving

PMOLED displays are driven one line at a time (line multiplexing). This means for a given average display brightness a peak brightness for the active line being a multiple of the number of lines is required. Driving with very high pulse currents has some disadvantages towards constant current mode (active-matrix/AMOLED) driving. Firstly, the current efficiency and the lifetime are reduced at very high currents. Furthermore the voltage drop (energy loss) on driving electronics and display wires increases. This is the reason, why very bright large-area PMOLED displays with more than 128 lines can be barely found until now. However, PMOLED displays are much cheaper to manufacture than AMOLEDs

Multi-line driving

To overcome the above mentioned challenges, a driving of multiple lines is supported by the driver. The underlaying algorithm decomposes the image information into multi-line matrices and efficiently reduces the driving current amplitude of the OLED pixels. The MLA mode uses multiple lines in parallel, thereby splitting the column current into several parts flowing through multiple OLEDs, which reduces the individual OLED peak current.

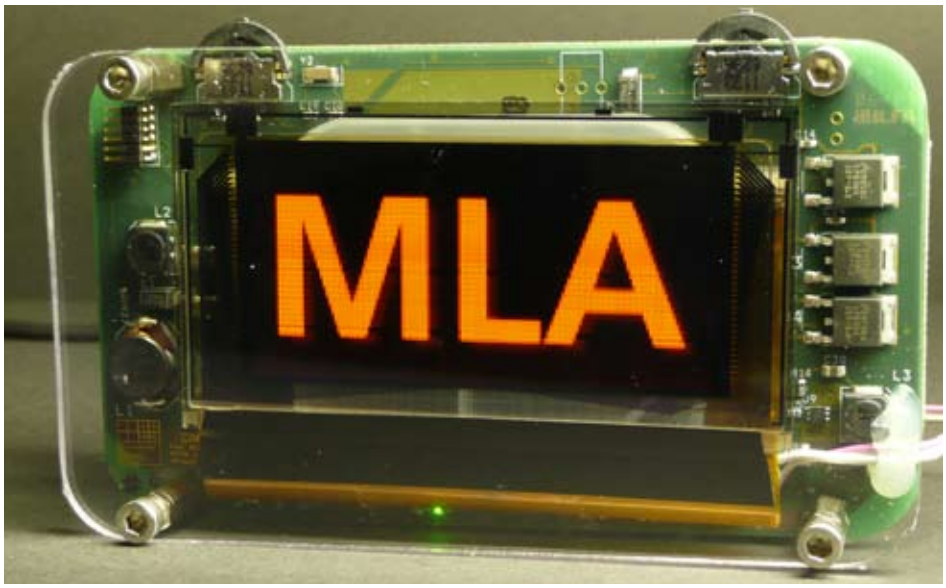

Fig. 1: OLED multiline driver demonstrator

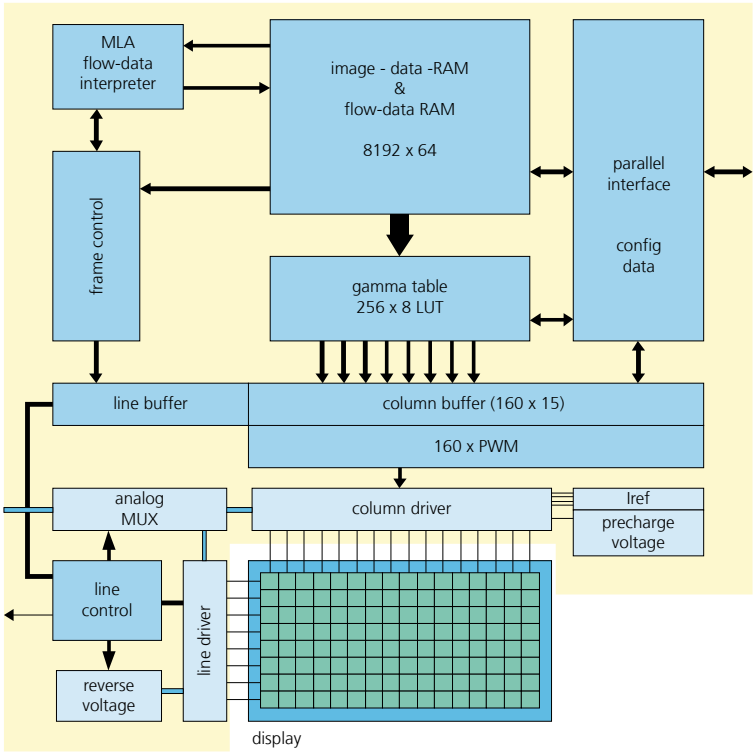

Fig. 2: Driver ASIC block diagram

Flow data interpretation

For supporting multi-line addressing (MLA) "flow data" which is the decomposed representation of the "normal" image, the frame control unit is able to handle line data with additional line specific header information. The column current is programmable in 128 steps depending on number of lines and MLA current reduction factor. In MLA mode the header data is interpreted and used for (multiple) line driving. Thereby the sequence of line driving can be programmed in any needed order. This is usable also for optimizing single line driving.

Internal characterization capabilities

Because of the development platform concept the ASIC contains supporting blocks for analog measurement. This means every internal row or column signal and current or temperature sensors can be mapped to two independent measurement outputs. The trigger output is programmable to every line number activation, phase, and clock number. This gives the ability to synchronize the measurement to any clock within one frame driving sequence.

Fig. 3: ASIC microphotograph

Driver ASIC

The driver ASIC prototype is fabricated in a commercial 0.18 µm high-voltage CMOS process (figure 3). It allows maximum parallel driving of four random lines (4-out-of-80), therefore is not limited to consecutive multiline addressing. The flow data interpreter allows maximum flexibility in testing different decomposition schemes. The actual die size of 13 x 6 mm² is mainly defined by the area for the high current drivers (2 mA @ 125°C). Size reduction is possible by optimizing chip ratio (pad limited design) or reduced driver strength depending on customer's specification.

Driver module

The ASIC has been mounted chip-on-board (COB) to achieve a fully operational module incorporating power supply, controller, driver, and plug-able 160 x 80 PMOLED display (see figure 1), that allows investigations on different displays or driving schemes at the same driver. A Chip-on-Glass (COG) device is currently in preparation.

Features:

- 160 columns, 80 rows
- Multiline driving (up to 4 parallel)
- ≤ 2 mA column current
- ≤ 160 mA row current
- Pulse & amplitude modulation
  - Gray scale 8 bit (PWM)
  - 160 column current DACs (7 bit)
- ≤ 25 V OLED display voltage
- Flow data / image buffer 64 kB
- Flexible configuration
- Self test & internal measurement capabilities
- 331 pin ASIC for COG mounting
- refresh rate ≤ 120 Hz (80 rows)
- -40 °C … 125 °C
- Gamma table

Acknowledgements

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